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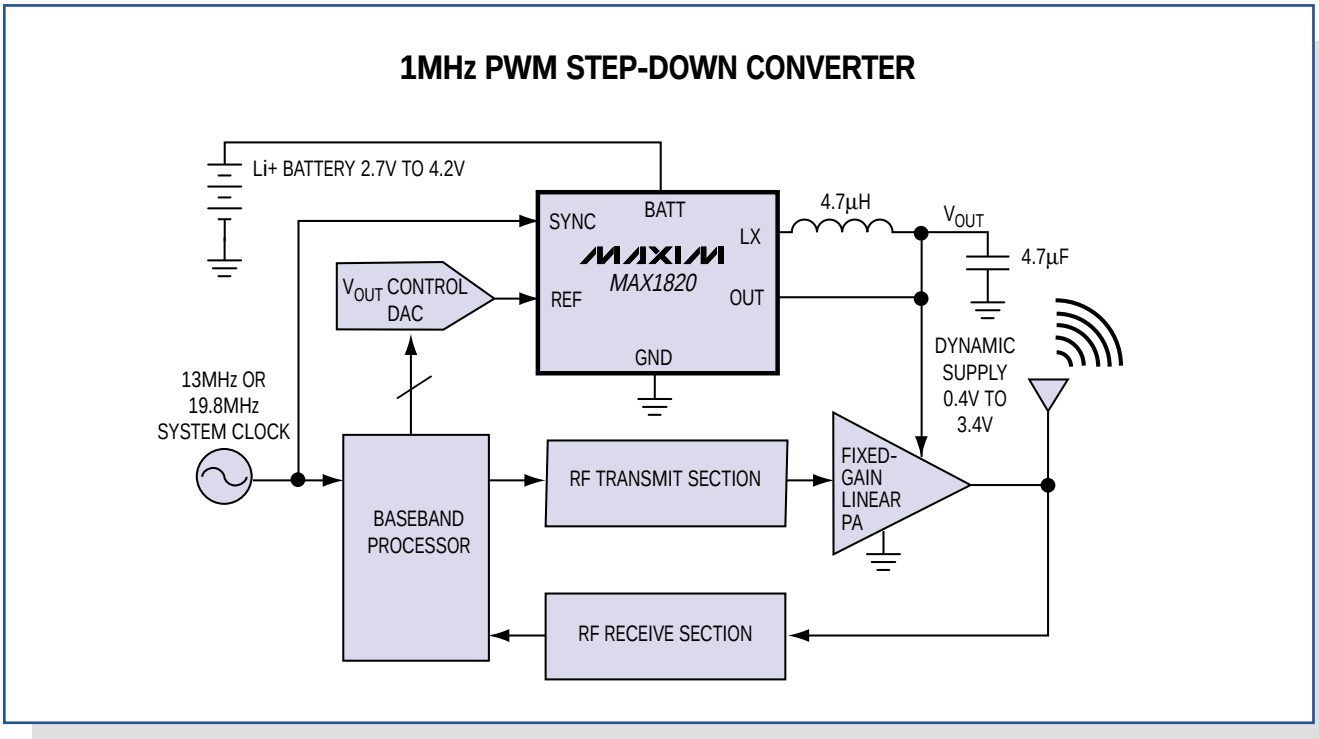


An efficient switching regulator like the MAX1820 dynamically adjusts the power-supply headroom of the WCDMA power amplifier (PA) in order to track the PA's transmit power and reduce wasted energy. (See article inside, page 3.)

News Briefs

MAXIM REPORTS RECORD REVENUES AND EARNINGS FOR THE THIRD QUARTER OF FISCAL 2001

Maxim Integrated Products, Inc., (Nasdaq: MXIM) reported record net revenues of $306.8 million for its fiscal third quarter ending March 31, 2001, a 35.4% increase over the $226.5 million reported for the same quarter a year ago. Net income increased to a record $103.9 million in the third quarter, compared to $74.7 million last year, a 39.1% increase. Diluted earnings per share were $0.33 for the third quarter, a 43.5% increase over the $0.23 reported for the same period a year ago.

During the quarter, cash and short-term investments increased by $89.0 million after paying $45.4 million for 770,000 shares of the Company's common stock and $65.3 million for property and equipment. Inventories decreased slightly. Gross margin for the third quarter was 71.4%, compared to 70.6% in the second quarter. Research and development expense was $52.1 million or 17.0% of net revenues in the third quarter, compared to $51.3 million or 16.8% of net revenues in the second quarter. During the quarter, the Company increased inventory reserves by $12.9 million and recorded a writedown of property and equipment of $13.5 million to cost of goods sold, $4.1 million to research and development expense, and $0.9 million to selling, general and administrative expense.

End market bookings in the third quarter of fiscal 2001 were $205 million, down from second quarter end market bookings of $332 million. No geographical or product area was spared. Turns orders received in the quarter were $51 million, compared to $58 million received in the prior quarter (turns orders are customer orders that are for delivery within the same quarter and may result in revenue within the same quarter if the Company has available inventory that matches those orders).

Third quarter ending backlog shippable within the next 12 months was approximately $296 million, including approximately $239 million requested for shipment in the fourth quarter of fiscal 2001. The Company's second quarter ending backlog shippable within the next 12 months was approximately $431 million, including approximately $330 million that was requested for shipment in the third quarter. All of these backlog numbers have been adjusted to be net of cancellations and estimated future U.S. distribution ship and debit pricing adjustments.

The Company completed its acquisition of Dallas Semiconductor Corporation on April 11, 2001. Dallas Semiconductor realized net revenues of $91.1 million and net income of $5.9 million in its quarter ended April 1, 2001. At the end of Q401, Maxim will begin reporting its results combined with those of its wholly owned subsidiary, Dallas Semiconductor.

Jack Gifford, Chairman, President, and Chief Executive Officer, commented on the third quarter results: "In this business environment of excess inventories and reduced consumption that has accompanied the decline of exaggerated dot-com and internet-related consumption, Maxim's third and fourth quarter results should outperform the industry. We expect much of the excess inventory to become obsolete as a new generation of communications equipment comes to market to meet the ever-increasing demand for data. Although the current downturn could prove to be atypical, our experience has shown that analog and mixed-signal companies typically go through later and less severe declines than their digital counterparts. Maxim's balance sheet remains strong."

Mr. Gifford continued: "Although order rates declined during the quarter as customers worked through their existing inventories, our turns order rate stabilized in the third quarter and has increased during the first part of the fourth quarter. We expect that our customers are getting a handle on actual inventories and are beginning to buy for near-term shortages as needed. The steepness of the order rate fall-off was certainly not expected, and we have spent considerable effort attempting to understand the drivers as well as its depth and duration as it relates to the next 12 months. We will post on our website (www.maxim-ic.com/info/commentary.htm) some of this analysis by equipment segment. While the increase in turns order rate is encouraging, we have limited visibility of future order levels. Our current estimate is that the combined revenues and earnings of Maxim and Dallas Semiconductor will decline in the fourth quarter from their pro forma combined results for the March 2001 quarter by 15 to 20 percent, prior to merger-related charges and conformance of accounting policies."

Mr. Gifford continued: "We are pleased that the Dallas Semiconductor merger was closed so promptly and that we are now able to work with management of our subsidiary to expand its business and bring its performance into line with Maxim's. We continue to be very impressed with the quality and commitment of Dallas personnel. During the fourth quarter, Dallas will aggressively merchandize over 40 products, many targeted for the T1, T3, fiber, network server/computer, and sensing markets. Although economic conditions are challenging at the present time, we are confident that our combined business will emerge from this period with a broad and attractive product line well positioned for future growth."

Improving transmit efficiency in 2.5G and 3G handsets

As the planned introduction of 3rd-generation (3G) cellular phones approaches, handset designers have been busy developing new solutions to accommodate the demands of high-speed data transmission. Among the greatest of these demands are software, screen technology, data-processing bandwidth, and the preservation of reasonable battery life. In 2nd-generation (2G) voice-only and low-data-rate handsets, the demands are not as great, allowing many simplifications and cost savings. A particular example of this is that the typical 2G handset's transmit power amplifier (PA) is powered directly from the battery for less than optimum efficiency. In 3G handsets, the transmission of high-speed data will require increased bandwidth and increased power at the antenna; therefore, a more efficient solution is required to maintain long battery life. One architecture now gaining widespread favor among cell-phone manufacturers uses a highly specialized step-down DC-DC switching regulator to power the PA.

The principle behind the use of a switching regulator is that the PA's supply voltage headroom can be dynamically adjusted to barely accommodate the RF signal amplitude in the PA (**Figure 1**). By efficiently doing this with a switching regulator, the battery power savings are greatest when operating at anything less than peak transmit power (**Figure 2**). Since peak power is only needed when the handset is very far away from the base station and/or transmitting data, the overall power savings are tremendous. If the PA supply voltage can be efficiently varied over a wide enough dynamic range, then a fixed-gain linear PA may be utilized, negating the need for a separate bias control signal (as presently used in 2G phones). Of course, a bias control signal may still be utilized for an added degree of control, and some cell-phone manufacturers are actively pursuing this topology.

Another major consideration to system performance is the specialized characteristics required of the step-down switching regulator. To understand the requirement, the PA must first be studied in terms of its load profile.

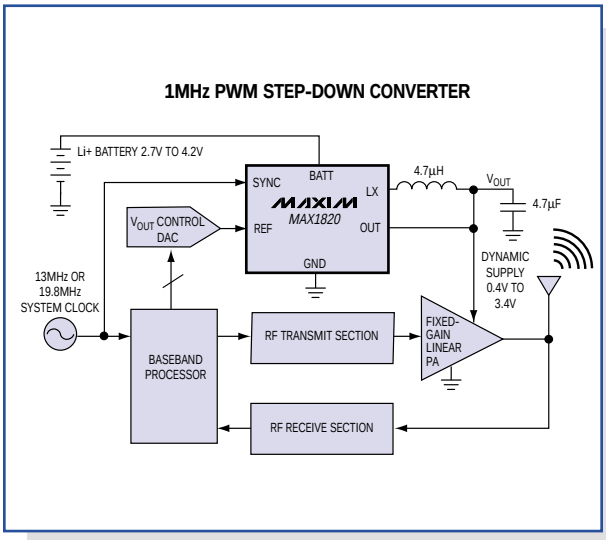


Figure 1. An efficient switching regulator like the MAX1820 dynamically adjusts the power-supply headroom of the WCDMA power amplifier (PA) in order to track the PA's transmit power and reduce wasted energy.

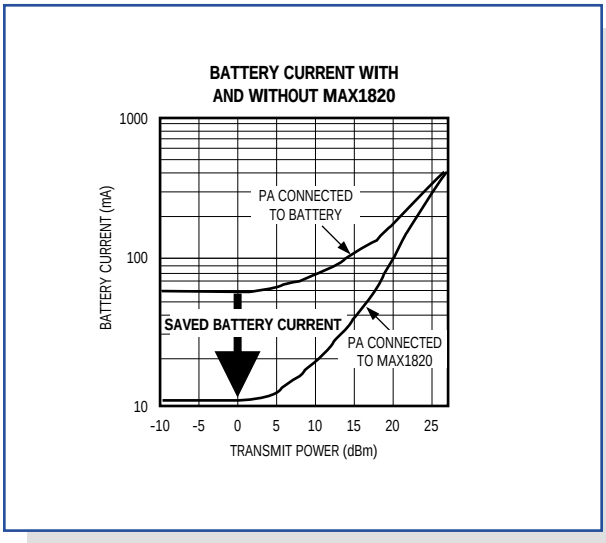


Figure 2. Compared to powering the PA directly from the battery, the use of the MAX1820 dramatically reduces the handset's battery current, especially at lower transmit power levels where the probability density is highest.

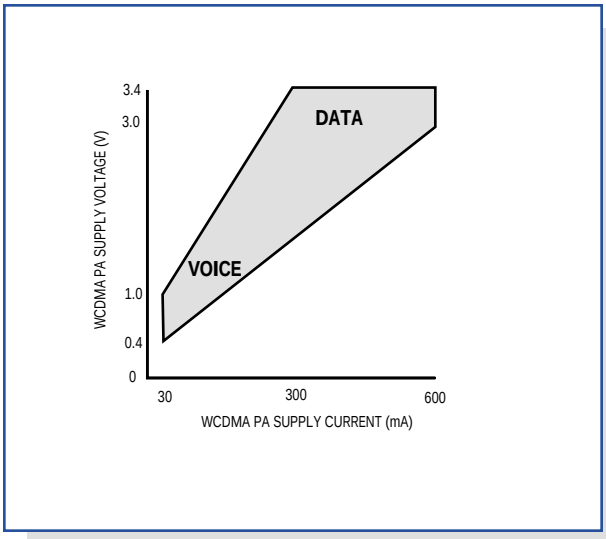


Figure 3. The typical load profile of a fixed-gain, bipolar WCDMA power amplifier has a significant resistive component. The supply voltage and current varies from as little as 0.4V at 30mA (12mW) to 3.4V at 600mA (2040mW).

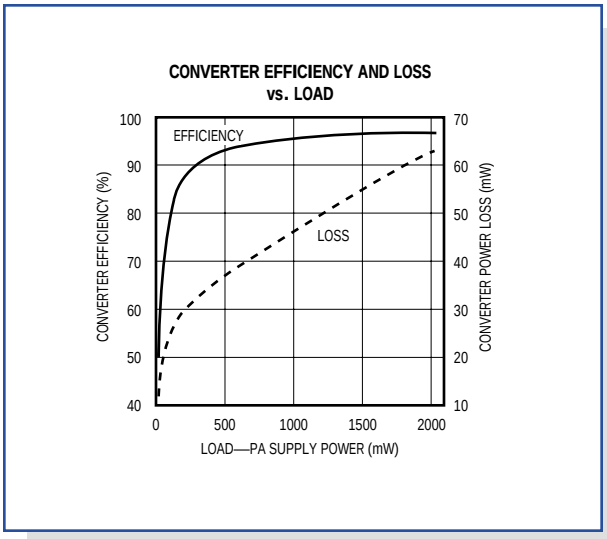


Figure 4. The MAX1820 step-down switching regulator is optimized for high efficiency over a very wide load range, even while maintaining constant fixed-frequency switching at 1MHz for low output ripple and noise.

Figure 3 was provided by a major cell-phone manufacturer and is the load profile for a bipolar, fixed-gain, WCDMA power amplifier. Under peak transmit power, the PA requires 3.4V supply rail and will draw between 300mA and 600mA. Under lowest transmit power, close to a base station and transmitting voice only, the PA draws as little as 30mA with supply voltage between 0.4V and 1V. This corresponds to PA power consumption of 2040mW maximum and 12mW minimum.

Optimization for this type of PA as a load is no trivial task for the switching regulator. The MAX1820 WCDMA cellular phone step-down regulator meets the requirements. Below is a list of the specific requirements that set the MAX1820 apart from other switching regulators:

- High Efficiency Over Wide Load—Without high efficiency, the expense of using a switching regulator is no longer justified; therefore, high efficiency and power savings were the dominant factors in the MAX1820 design (**Figure 4**). During data transmission (approximately 500mW to 2040mW), the low 0.15Ω on-resistance of the MAX1820's PFET power switch provides up to 97% efficiency. During voice transmission (approximately 12mW to 500mW), the MAX1820's internal 0.2Ω NFET synchronous rectifier and low supply current of 3.3mA (in forced-PWM mode) provide about 90% efficiency. Although 90% efficiency sounds good, it is an exceptional performance for light-load efficiency while switching at a constant 1MHz, as illustrated by the low converter power loss shown in Figure 3. This performance can be attributed to careful design and the use of submicron geometry fabrication for a low gate capacitance at a given FET on-resistance.
- Dynamic Output Voltage Adjustment—The output voltage needs to be adjustable between 3.4V and 0.4V. To accomplish this, an analog control pin, REF, on the MAX1820 is driven by a digital-to-analog converter (DAC). Because the DAC's output voltage range does not extend to 3.4V, the voltage gain of the converter from REF to OUT is 1.76.
- Fast 30µs Output Slew Rate and Settling—In the WCDMA system architecture, transmit power is adjusted up or down by 1dB every 666µs as requested by the base station. Additionally, the handset may enter or exit data-transmission mode every 10ms, corresponding to a large-scale transmit power change (**Figure 5**). All transmit power level changes need to be completed within 50µs; however, the time for the switching regulator to change PA supply power is less than this to accommodate any system latency in the baseband and DAC. For this reason, the MAX1820 was specifically designed to slew and settle its output voltage in less than 30µs, even for full-scale changes in voltage and current. Because the output must slew quickly, the MAX1820 is limited to only 4.7µF of output capacitance, making stable switching more of a challenge. The added benefit of the 4.7µF capacitor

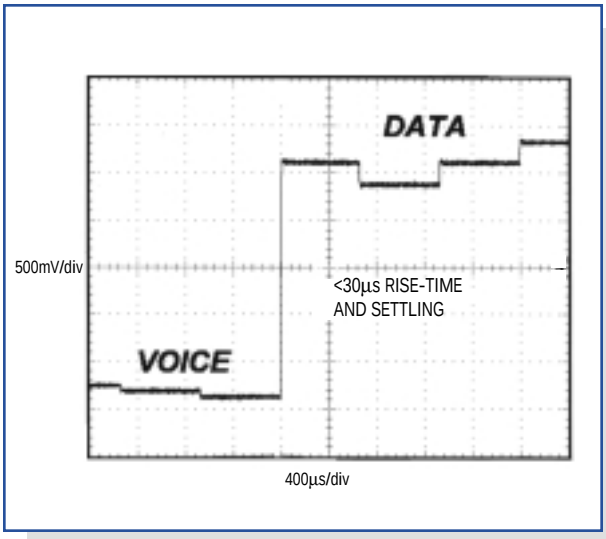


Figure 5. The MAX1820's output power is dynamically adjusted in 1dB increments every 666µs to track the WCDMA PA transmit power level. However, when changing from voice mode into data mode (or the reverse), the MAX1820 may be required to provide a full-scale change in output voltage and load current. All changes in output voltage must be settled within 30µs to maintain linearity in the PA.

is that a low-ESR ceramic type will provide low output ripple of about 5mVp-p. Another issue for the step-down regulator occurs when transmit power needs to be rapidly reduced, such as when exiting data mode. In this case, the MAX1820 reverses inductor current and pulls the output voltage down to maintain the 30µs settling time. If this were not done, the PA's linearity would change as its supply voltage slowly decayed on its own. Also, this technique actually saves power by transferring previously stored energy on the output capacitor back to the battery at the MAX1820's input.

- Stable 9.5% to 100% PWM Duty Cycle and Low Dropout—Assuming the handset is powered from a single lithium-ion (Li+) battery cell, the expected input voltage range for the switching regulator is 4.2V to 2.7V. Because constant fixed-frequency switching is desired for predictable noise spectrum and low output ripple, the forced-PWM operation of the MAX1820 remains stable down to 9.5% duty cycle when the battery is fully charged at 4.2V and the required PA supply voltage is 0.4V. In itself this is not so difficult, but in conjunction with the opposite extreme, a discharged battery and high-power data transmission, the duty cycle must also extend fully to 100% and low dropout operation. To obtain very low dropout, the MAX1820's PFET is slightly oversized for very low 0.15Ω on-resistance. Assuming 0.1Ω series resistance in the inductor, the combined dropout is only 150mV at 600mA load, and proportionally less at lighter loads. According to the cell-phone manufacturers, it is acceptable that the data transmit range is somewhat reduced when the battery is discharged below 3.4V. Removing this concession would require an expensive, less-efficient buck-boost regulator.
- 1MHz Switching and Synchronization—The MAX1820 has an internal 1MHz oscillator to control the PWM switching frequency. Faster frequency would be a means of decreasing the external component sizes, but efficiency would be reduced to unacceptable levels. As stated earlier, utilizing fixed-frequency PWM provides a predictable noise spectrum and low output ripple. The MAX1820's 1MHz internal clock is also relatively accurate with only ±20% tolerance; however, for exact synchronization to the system clock in the handset, the MAX1820 includes a divide-by-13 (or divide-by-18) clock synthesizer which can be fed a 13MHz (or 19.8MHz) low-amplitude sine wave.

Conclusion

As the efficiency benefits of utilizing a step-down switching regulator to power a WCDMA PA are proven, this topology may be adopted across more 3G standards and a variety of end equipment, helping to make the promise of small, feature-laden data handsets and wireless mobile computing a reality.

The ABCs of ADCs: understanding how ADC errors affect system performance

Using a 12-bit resolution analog-to-digital converter (ADC) does not necessarily mean that your system will have 12-bit accuracy. Sometimes, much to the surprise and consternation of engineers, a data-acquisition system will exhibit much lower performance than expected. When this is discovered after the initial prototype run, a mad scramble for a higher performance ADC ensues, and many hours are spent reworking the design as the deadline for preproduction builds quickly approaches. What happened? What changed from the initial analysis? A thorough understanding of ADC specifications will reveal subtleties that often lead to less-than-desired performance. Understanding ADC specifications will also help you select the right ADC for your application.

System requirements

We assume that the overall system will have a total error budget based on the summation of error terms for each circuit component in the signal path. This root-mean-square (RMS) error budget is given by:

$$\text{Total error} = \sqrt{(E_1^2 + E_2^2 + E_3^2 + ... + E_N^2)} \qquad (1)$$

where E_N represents the term for a particular circuit component. In this example, let's assume we need 0.1% or 10 bits of accuracy, so it makes sense to choose a converter with greater resolution than this. If we select a 12-bit converter, we can assume it will be adequate; but without reviewing the specifications, there is no guarantee of 12-bit performance (it may be better or worse). For example, a 12-bit ADC with 4LSB of integral nonlinearity error (INL) can give only 10 bits of accuracy at best (assuming the offset and gain errors have been calibrated). A device with 0.5LSB of INL can give 0.0122% error or 13 bits of accuracy (with gain and offset errors removed). To calculate best-case accuracy, divide the maximum INL error by 2N, where N is the number of bits. In our example, allowing 0.075% error (or 11 bits) for the ADC leaves 0.025% error for the remainder of the circuitry, which will include errors from the sensor, the associated front-end signal conditioning circuitry (op amps, multiplexers, etc.), and possibly digital-to-analog converters (DACs), PWM signals, or other analog output signals in the signal path.

We will also assume that we are measuring a slow-changing, DC-type, bipolar input signal with a 1kHz bandwidth and that our operating temperature range is 0°C to +70°C with performance guaranteed from 0°C to +50°C.

DC performance

Differential nonlinearity

Though not mentioned as a key parameter for an ADC, the differential nonlinearity (DNL) error is the first specification to observe. DNL reveals how far a code is from a neighboring code. The distance is measured as a change in input-voltage magnitude and then converted to LSB **(Figures 1a, 1b, 1c, 1d)**. INL is the integral of the DNL errors, which is why DNL is not included in our list of key parameters. The key for good performance for an ADC is the claim "no missing codes." This means that as the input voltage is swept over its range, all output code combinations will appear at the converter output. A DNL error of less than ±1LSB guarantees no missing codes (Figure 1a). In Figures 1b, 1c, and 1d, three DNL error values are shown. With a DNL error of -0.5LSB (Figure 1b), the device is guaranteed to have no missing codes. With a value equal to -1LSB (Figure 1c), the device is not necessarily guaranteed to have no missing codes (Code 10 is missing). However, most ADCs that specify a maximum DNL error of ±1LSB will specifically state whether the device has missing codes or not. Because the production test limits are actually tighter than the data sheet limits, it is usually guaranteed to have no missing codes. With a DNL value greater than -1LSB (-1.5LSB in Figure 1d), the device has missing codes.

When DNL-error values are offset (that is, -1LSB, +2LSB), the ADC transfer function is altered. Offset DNL values can still, in theory, have no missing codes. The key is having -1LSB as the low limit. DNL is measured in one direction, usually going up the transfer function. The input-voltage level required to create the transition at code [N] is compared to that at code [N + 1]. If the difference is 1LSB, the DNL error is zero. If it is greater than 1LSB, the DNL error is positive; if it is less than 1LSB, the DNL error is negative.

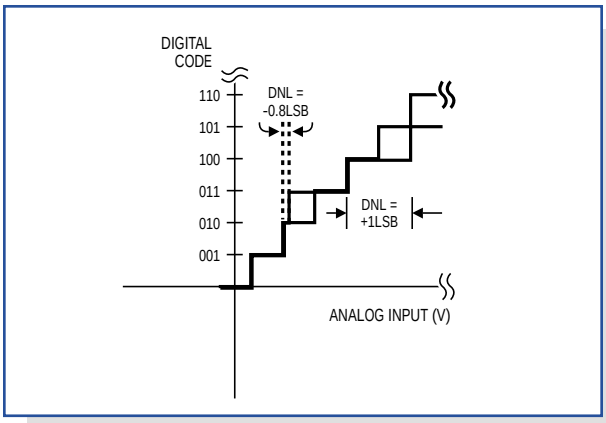


Figure 1a. DNL error: no codes are missing.

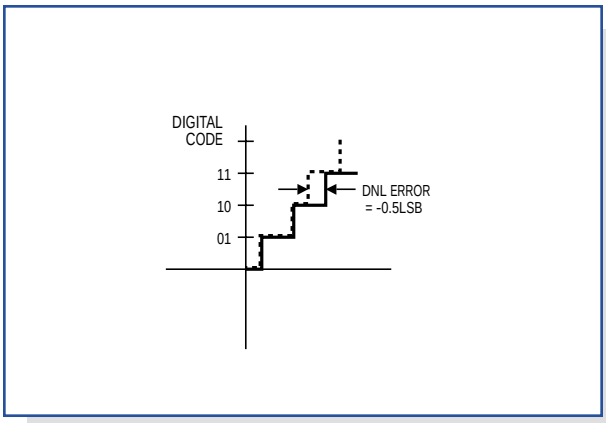


Figure 1b. DNL error: no codes are missing.

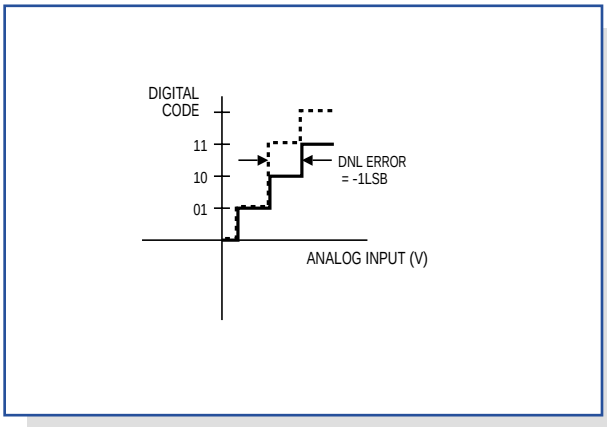


Figure 1c. DNL error: Code 10 is missing.

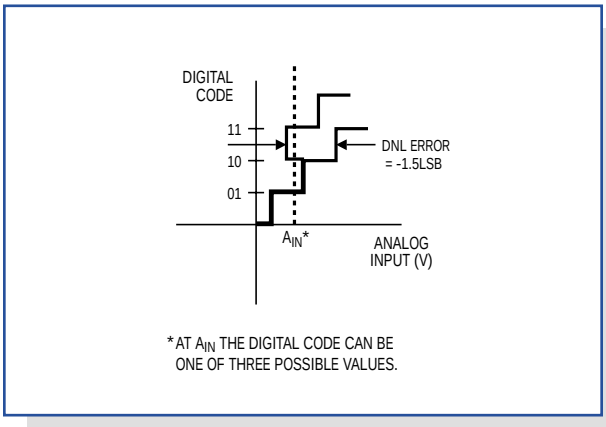


Figure 1d. DNL error: When the input voltage is swept, Code 10 will be missing.

Having missing codes is not necessarily bad. If you need only 13 bits of resolution and you have a choice between a 16-bit ADC with a DNL specification ≤ ±4LSB DNL (which is effectively 14 bits, no missing codes) that costs $5, and a 16-bit ADC with a DNL of ≤ ±1LSB that costs $15, then buying the lower grade version of the ADC will allow you to greatly reduce component cost and still meet your system requirements.

Integral nonlinearity

Integral nonlinearity (INL) is defined as the integral of the DNL errors. The INL error tells how far away the measured converter result is from the ideal transfer-function value. Continuing with our example, an INL error of ±2LSB in a 12-bit system means the maximum nonlinearity error may be off by 2/4096 or 0.05% (which is already about two-thirds of the allotted ADC error budget). Thus, a 1LSB (or better) part is required. With a ±1LSB INL error, the accuracy is 0.0244%, which accounts for 32.5% of the allotted ADC error budget. With a specification of 0.5LSB, the accuracy is 0.012%, and this accounts for only about 16% (0.012%/0.075%) of our ADC error budget limit. Note that neither INL nor DNL errors can be calibrated or corrected easily.

Offset and gain errors

Offset and gain errors can easily be calibrated out using a microcontroller (µC) or a digital signal processor (DSP). With offset error, the measurement is simple when the converter allows bipolar input signals. In bipolar systems, offset error shifts the transfer function but does not reduce the number of available codes (**Figure 2**). There are two methodologies to zero out bipolar errors. In one, you shift the x and y axes of the transfer function so that the negative full-scale point aligns with the zero point of a unipolar system (**Figure 3a**). With this technique, you simply remove the offset error and then adjust for gain error by rotating the transfer function about the “new”

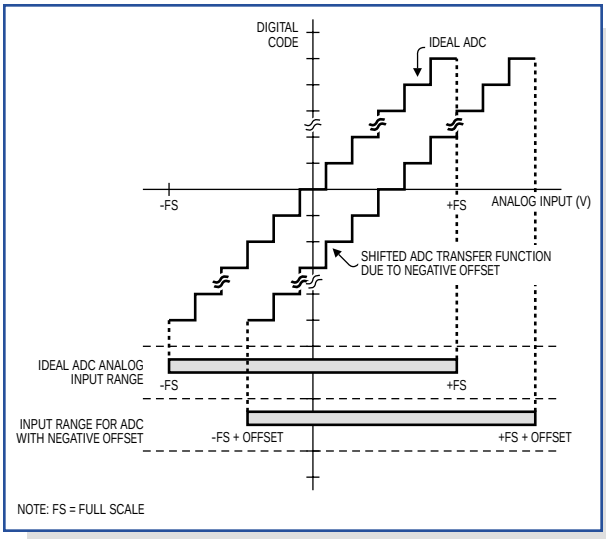


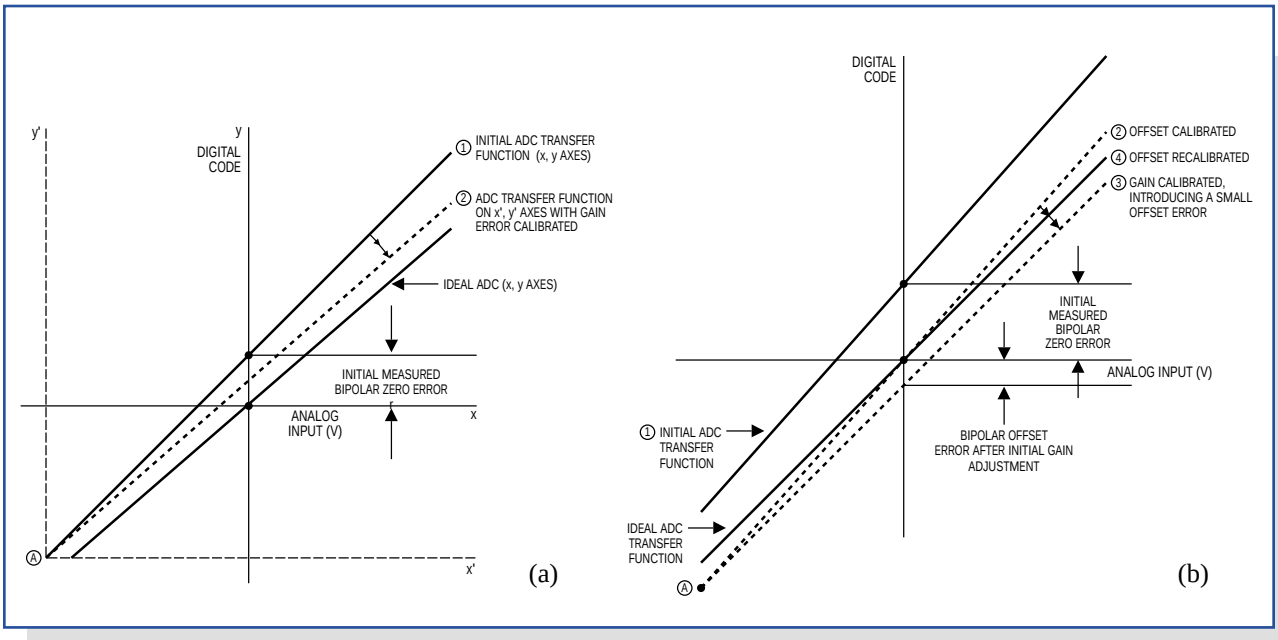
Figure 2. This offset is shown in a bipolar system.

zero point. The second technique entails using an iterative approach. First apply 0V to the ADC input and perform a conversion; the conversion result represents the bipolar zero-offset error. Then perform a gain adjustment by rotating the curve about the negative full-scale point (**Figure 3b**). Note that the transfer function has pivoted around point A, which moves the zero point away from the desired transfer function. Thus, a subsequent offset-error calibration may be required.

Unipolar systems are more complicated. If the offset is positive, use the same methodology as that for bipolar supplies. The difference here is that you lose part of the ADC's range (**Figure 4**). If the offset is negative, you cannot simply do a conversion and expect the result to represent the offset error. Below zero, the converter will just display zeros. Thus, with a negative offset error, you must increase the input voltage slowly to determine where the first ADC transition occurs. Here, again, you lose part of the ADC range.

Returning to our example, two scenarios for offset error are given below.

1. If the offset error is +8mV with a 2.5V reference, this corresponds to 13LSB of error for a 12-bit ADC (8mV/[2.5V/4096]). Though the resolution is still 12 bits, you must subtract 13 codes from each conversion result to compensate for the offset error. The actual, measurable, full-scale value in this scenario is now 2.5V (4083/4096) = 2.492V. Any value above this will over-range the ADC. The dynamic range, or range of input values, for the ADC has been reduced. This is even more important for higher-resolution ADCs; 8mV represents 210LSB at the 16-bit level (V_{REF} = 2.5V).
2. If the offset is -8mV (assuming a unipolar input), small analog-input values near zero will not register when a conversion is performed until the analog input exceeds +8mV. This, too, reduces the dynamic range of the ADC.



Figures 3a and 3b. Calibrating bipolar offset error. (Note: The stair-step transfer function has been replaced by a straight line, because this graph shows all codes, and the step size is so small that the line appears to be linear.)

Gain error is defined as the full-scale error minus the offset error (**Figure 5**). Full-scale error is measured at the last ADC transition on the transfer-function curve and compared against the ideal ADC transfer function. Gain error is easily corrected in software with a linear function y = (m1/m2)(x), where m1 is the slope of the ideal transfer function and m2 is the slope of the measured transfer function (Figure 5).

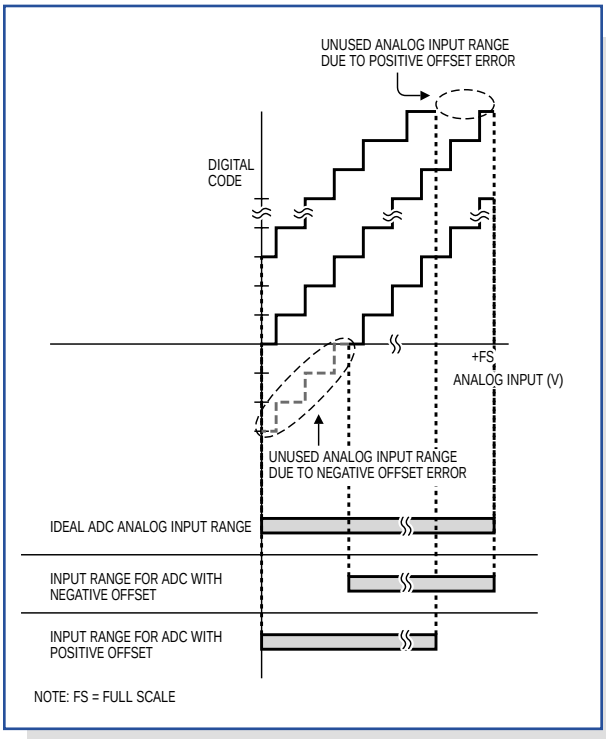


Figure 4. This offset error is shown in a uniploar system.

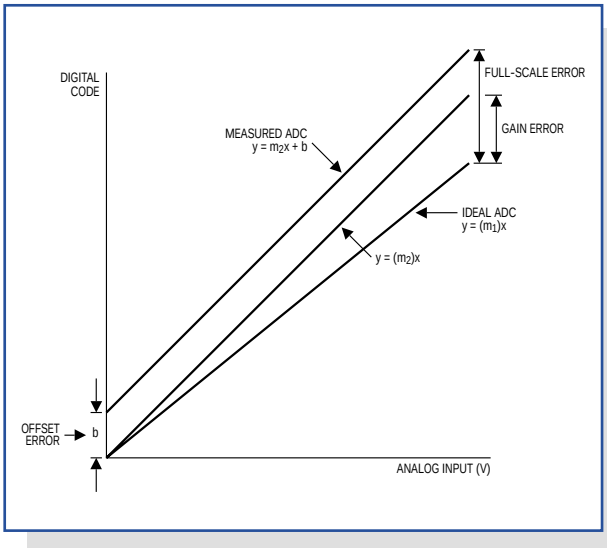


Figure 5. Gain error is defined as the full-scale error minus the offset error.

The gain-error specification may or may not include errors contributed by the ADC's voltage reference. In the electrical specifications, it is important to check the conditions to see how gain error is tested and to determine whether it is performed with an internal or external reference. Typically, the gain error is much worse when an on-chip reference is used. If the gain error were zero, when a conversion were performed the conversion result would begin to yield all ones (3FFh in our 12-bit example) when the full-scale analog input were applied (**Figure 6**). As our converter is not ideal, you can initially end up with all ones in the conversion result when a voltage greater than full scale is applied (negative gain error) or when a voltage less than full scale is applied (positive gain error). Two ways to adjust for gain error are to either tweak the reference voltage so that at a specific reference-voltage value the output gives full scale, or use a linear correction curve in software to change the slope of the ADC transfer-function curve (a first-order linear equation or a lookup table can be used).

As with offset error, you lose dynamic range with gain error. For example, if a full-scale input voltage is applied and the code obtained is 4050 instead of the ideal 4096 (for a 12-bit converter), this is defined as negative gain error, and in this case the upper 46 codes will not be used. Similarly, if the full-scale code of 4096 appears with an input voltage less than full scale, the ADC's dynamic range is again reduced (Figure 6). With positive full-scale errors you cannot calibrate beyond the point where the converter gives all ones in the conversion result.

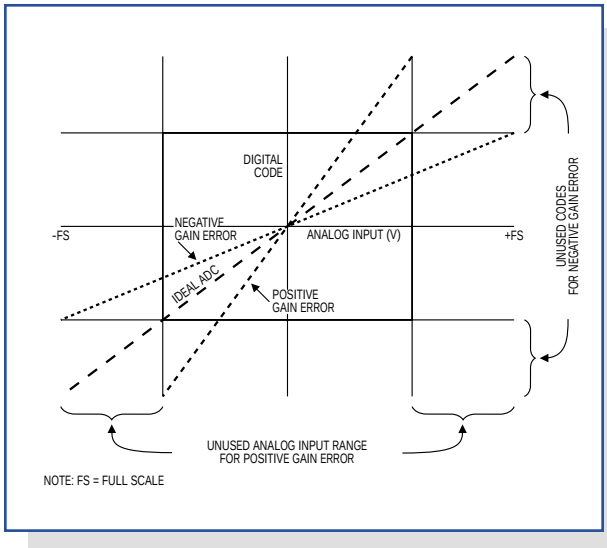


Figure 6. Gain error reduces dynamic range.

The easiest way to handle offset and gain errors is to find an ADC with values low enough so that you don't have to calibrate. It's fairly easy to find 12-bit ADCs with offset and gain errors less than 4LSB.

Other subtle error sources

Code-edge noise

Code-edge noise is the amount of noise that appears right at a code transition on the transfer function. It is often not specified in the data sheet. Even in higher resolution converters (16+ bits), where code-edge noise is much more prevalent due to the smaller LSB size, it is often not specified. Sometimes code-edge noise can be several LSB. Conversions performed with the analog input right at the code edge can result in code flicker in the LSB. Significant code-edge noise means that an average of samples must be taken to effectively remove this noise from the converter results. How many samples are needed? If the code-edge noise is $2/3LSB_{RMS}$, this equates to approximately 4LSBp-p. Sixteen samples will have to be taken to reduce the noise to 1LSBp-p (the square root of the number of samples determines the improvement in performance).

The reference

One of the biggest potential sources of errors in an ADC with an internal or external reference is the reference voltage. Often, if the reference is included on-chip, it is not specified adequately. To understand the source of the reference errors, it is important to look at three specs in particular: temperature drift, voltage noise, and load regulation.

Temperature drift

Temperature drift is the most overlooked specification in the data sheet. As an example, note how temperature drift affects the performance of an ADC based on resolution (**Figure 7**). For a 12-bit converter to maintain accuracy over the extended temperature range (-40°C to +85°C), the drift must be a maximum of 4ppm/°C. Unfortunately, no ADC is available with this kind of on-chip reference performance. If we relax the requirements, a 10°C temperature excursion means the 12-bit ADC reference can drift no more than 25ppm/°C, which again is a fairly tight requirement for on-chip references. Prototyping frequently does not reveal the significance of this error because parts are often from a similar lot. Thus, the test results do not take into account the extremes that occur in specs due to manufacturing-process variations.

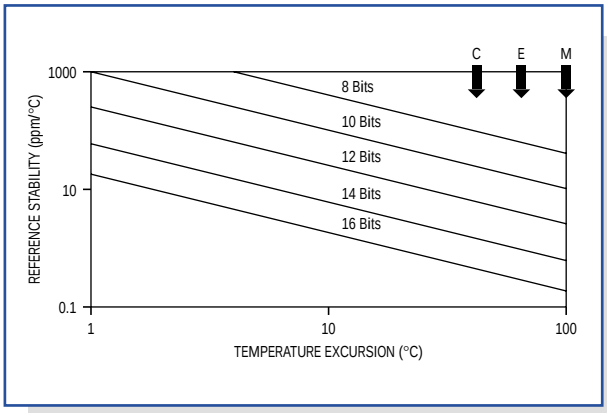


Figure 7. Voltage-reference drift requirements relate to ADC resolution.

For some systems, the reference accuracy is not a big issue, as the temperature is held constant, eliminating the drift problem. Some systems use a ratiometric measurement, where the reference errors are removed because the same signal that excites the sensor is used as the reference voltage (**Figure 8**). Because the excitation source and reference move as one, drift errors are eliminated.

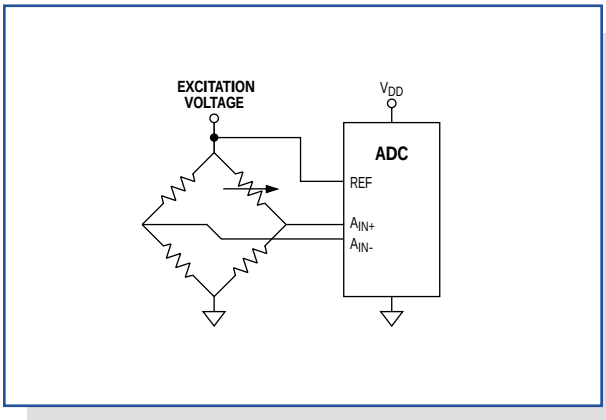


Figure 8. Ratiometric ADC conversion eliminates drift noise.

In other systems, calibration is performed often enough that reference drift is effectively removed. In still other systems, absolute accuracy is not critical, but relative accuracy is. Therefore, the reference can drift slowly with time and the system will provide the desired accuracy.

Voltage noise

Another important spec is voltage noise. It is often specified as either an RMS value or a peak-to-peak value. Convert the RMS value to a peak-to-peak value to evaluate its effect on performance. If a 2.5V reference has 500µV of peak-to-peak voltage noise at the output (or $83\mu V_{RMS}$), this noise represents 0.02% error or barely

12-bit performance, and this is before any of the converter errors are considered. Ideally, our reference-noise performance should be a small fraction of an LSB so not to limit the ADC's performance. ADCs with on-chip references usually don't specify voltage noise, so it is up to the user to determine the error. If you are not getting the performance you desire and are using an internal reference, try using a very good external reference to determine if the on-chip reference is in fact the culprit.

Load regulation

The final spec is reference load regulation. Often the voltage reference used for an ADC has ample current to drive other devices, so it is used by other ICs.

The current drawn by those other components will affect the voltage reference, which means that as more current is drawn the reference voltage will droop. If the devices using the reference are turning on and off intermittently, the result will be a reference voltage that moves up and down. A 0.55µV/µA reference-load-regulation specification for a 2.5V reference means that if other devices draw 800µA, the reference voltage will change up to 440µV, which is 0.0176% (440µV/2.5V) or almost 20% of the available error margin.

Other temperature effects

Two specifications that are often given little attention are offset drift and gain drift. These specs are usually given as typical numbers only, leaving it up to the users to determine if the specification is good enough for their system requirements. Offset- and gain-drift values can be compensated in a couple of different ways. One way is to fully characterize the offset and gain drift, and provide a lookup table in memory to adjust the values as temperature changes. This, however, is a cumbersome process, as each ADC must be compensated individually and the compensation process is a time-consuming effort. The second method is to perform calibrations when a significant temperature change has occurred.

With systems that do a one-time temperature calibration, it's important to pay heed to the drift specs. If the initial offset is calibrated and the temperature moves, there will be an error introduced due to the drift term that can negate the effects of the calibration. For example, assume a reading is done at temperature X. Some time later, the temperature has changed 10°C and the exact same measurement is taken. These two readings can give different results, calling into question the repeatability and thus the reliability of the system.

There is a good reason why manufacturers do not give maximum limits. This increases the cost. Drift testing requires special boards, and an extra step must be added to the test flow (which equates to an additional manufacturing cost) to make sure that the parts do not exceed the maximum-drift limit.

Gain drift is more of an issue, particularly for devices tested with an internal reference. In this case, the reference drift can be included in the gain-drift parameter. For an external reference, the IC's gain drift is typically small, like 0.8ppm/°C. Thus, a ±10°C temperature change results in a ±8ppm change. For example, 12-bit performance equates to 244ppm (1/4096 = 0.0244% = 244ppm). So in ±8ppm we see an error that represents only a fraction of an LSB at the 12-bit level.

AC performance

Some ADCs perform well only with input signals at or near DC. Others perform well with input signals from DC up to Nyquist. Just because DNL and INL meet the system requirements does not mean that the converter will give that same performance when AC signals are considered. DNL and INL are DC tests. We must look to the AC specs to get a good feeling for AC performance. The electrical characteristics table and the typical operating characteristics found in the data sheet offer clues to the AC performance. The key specs to review are signal-to-noise ratio (SNR), signal-to-noise and distortion ratio (SINAD), total harmonic distortion (THD), and spurious-free dynamic range (SFDR). The first specification to review is SINAD or SNR. SINAD is defined as the ratio of the RMS value of an input sine wave to the RMS value of the noise of the converter (from DC to the Nyquist frequency, including harmonic [total harmonic distortion] content). Harmonics occur at multiples of the input frequency (**Figure 9**). SNR is similar to SINAD, except that it does not include the harmonic content. Thus, the SNR should always be better than the SINAD. Both SINAD and SNR are typically expressed in dB. Quantization produces errors, and for an ideal ADC:

$$SINAD = [6.02\ (N) + 1.76]\ (dB) \quad (2)$$

where N is the number of bits. For an ideal 12-bit converter, the SINAD is 74dB. Should this equation be rewritten in terms of N, it would reveal how many bits of information are obtained as a function of the RMS noise:

$$N = (SINAD - 1.76)/6.02 \quad (3)$$

This equation is the definition for effective number of bits, or ENOB.

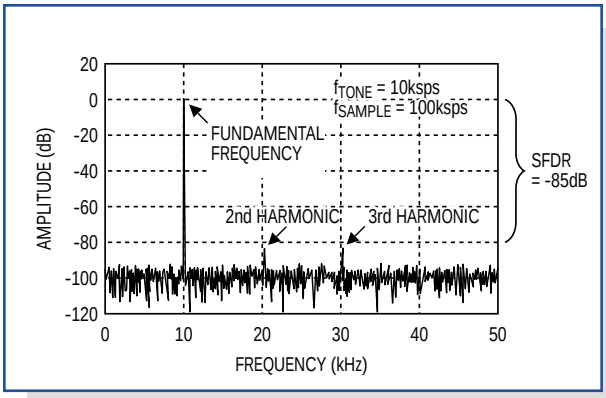


Figure 9. FFT plot reveals AC performance of an ADC.

SINAD is a function of the input frequency. As frequency increases toward the Nyquist limit, SINAD decreases. If the specification in the data sheet is tested at low frequencies compared to the Nyquist frequency, the performance will be much worse near Nyquist. Look for an ENOB graph in the typical operating characteristics of the data sheet. ENOB degrades with frequency primarily because THD gets increasingly worse as the input frequency increases. For example, with a SINAD minimum value of 68dB at the frequency of interest, you obtain an ENOB value of 11. Therefore, you have lost 1 bit of information due to the converter's noise and distortion performance. This means that your 12-bit converter can provide only 0.05% accuracy at best. Remember that INL is a DC spec; ENOB is the specification that tells about nonlinearities for AC signals.

SNR is the signal-to-noise ratio with the distortion components removed. SNR reveals where the noise floor of the converter is. There can be a steep decrease in SNR as a function of input frequency, which means the converter was not designed for frequencies near this point. One way to improve SNR is to oversample, which provides a processing gain. Oversampling is a method of lowering the noise floor of the converter by sampling at a rate much higher than the signal of interest. This spreads the noise out over a wider range in the frequency domain, thereby effectively reducing the noise at any one frequency bin. A 2x oversampling reduces the noise floor by 3dB.

SFDR is defined as the ratio of the RMS value of an input sine wave to the RMS value of the largest spur observed in the frequency domain using an FFT plot. It is typically expressed in dB. SFDR is important in certain communication applications that require maximizing the dynamic range of the ADC. Spurs prevent the ADC from converting small input signals, because the distortion component can be much larger than the signal of interest. This limits the dynamic range of the ADC. A large spur in the frequency domain may not significantly affect the SNR, but will significantly affect the SFDR.

Final thoughts

Returning to the ADC example, assume we are measuring DC-type signals and our ADC accepts bipolar input signals. We choose the B grade of the MAX1241, which has 1LSB DNL error, 1LSB INL error (0.0244%), 3LSB offset error (3/4096 = 0.0732%), and gain of 4LSB (0.0977%). Adding the errors, we obtain a total error of 0.1953%. We can calibrate out the offset and gain errors, dropping our error to 0.0244%. As long as our voltage-reference error is less than 0.075% - 0.024% = 0.051%, we are within the error budget. A 5ppm/°C drift of more than 50°C equates to a 0.025% drift error, with a 0.026% error budget remaining. For 12-bit performance, we need to have a voltage reference with a voltage-noise specification considerably less than 1LSB (which is 2.5V/4096 = 610µVp-p or 102µV_{RMS}). The MAX6166 is a good choice with 5ppm/°C drift and 30µV_{RMS} wideband voltage noise. It also has ample source and sink current capability to drive the ADC (and additional circuitry if needed). The 30µV noise spec equates to 180µVp-p, which is one-third of an LSB at the 12-bit level and one-sixth of an LSB at the 11-bit level (which is our actual system requirement).

A quick check of the MAX1241 gain drift reveals a specification of 0.25ppm/°C or 12.5ppm over a 50°C temperature change, which is well within spec.

Now we have a viable solution that should prevent any hidden performance hiccups due to the specifications. For this example we didn't address the AC performance. However, with your better understanding of the ADC specs and how they relate to the converter's performance, you will be armed with enough information to select the ADC that will give you the performance you need.

Fan control advances: consider fan regulation

Control of brushless DC fan motors can take on several forms. The simplest method is on/off switching with a single transistor. Linear regulators or power op amps can be combined with DACs to make variable-speed fan-control systems that are digitally programmable. PC health monitor ICs have offered DACs with an output that can be applied to an amplifier for driving a fan. PWM fan control chips are available that still require a DAC for digital interface, and PWM methods have to be used with some caution. The newest developments for fan control are complete digital interface ICs with complete fan driver circuits (except for the power transistor), which include the MAX1669. The MAX6650/MAX6651 take the forefront in advanced fan control because these devices are truly fan-speed regulators.

The MAX1669 represents the most common type of fan control available providing either a linear DAC output or a PWM output. The MAX1669 stands out because it includes a remote-junction temperature sensor on-board that can be connected to ICs equipped with sensing junctions or bipolar transistors such as 2N3904s used as sensors. The circuit of **Figure 1** is an example of the MAX1669 used for linear control of a fan. The MAX1669 is especially suited in situations where the fan cannot be equipped with a tachometer output because of either cost or technical requirements.

Fan control problems and solutions

A big problem in fan control is the nonlinear behavior of the fan with respect to input voltage. As shown in **Figure 2**, the typical fan does not even begin to rotate until a voltage between 3V and 8V is applied, depending on the fan. And even for a given fan, this exact voltage is subject to variations from fan to fan, and with temperature and age. When using a part such as the MAX1669, with simple fan driver amplifiers or PWM output, fans must be commanded to full speed briefly before programming low speeds. It is difficult to predict, and subject to wide variation, just how low the low speed can be. With lengthy evaluation, a minimum could be found for any fan. Regardless of the programmed speed of the fan, this is an open-loop system that does not regulate fan speed.

This lack of predictability of threshold voltages has given birth to some "Rube Goldberg" schemes among some of the fan control ICs. For instance, one IC examines whether or not the fan is rotating, and if it isn't, it raises the drive incrementally. If the fan still isn't rotating, it raises it another increment and so on until the fan starts.

The MAX1669, along with a tachometer feedback amplifier, offers a "clean" solution to this problem by

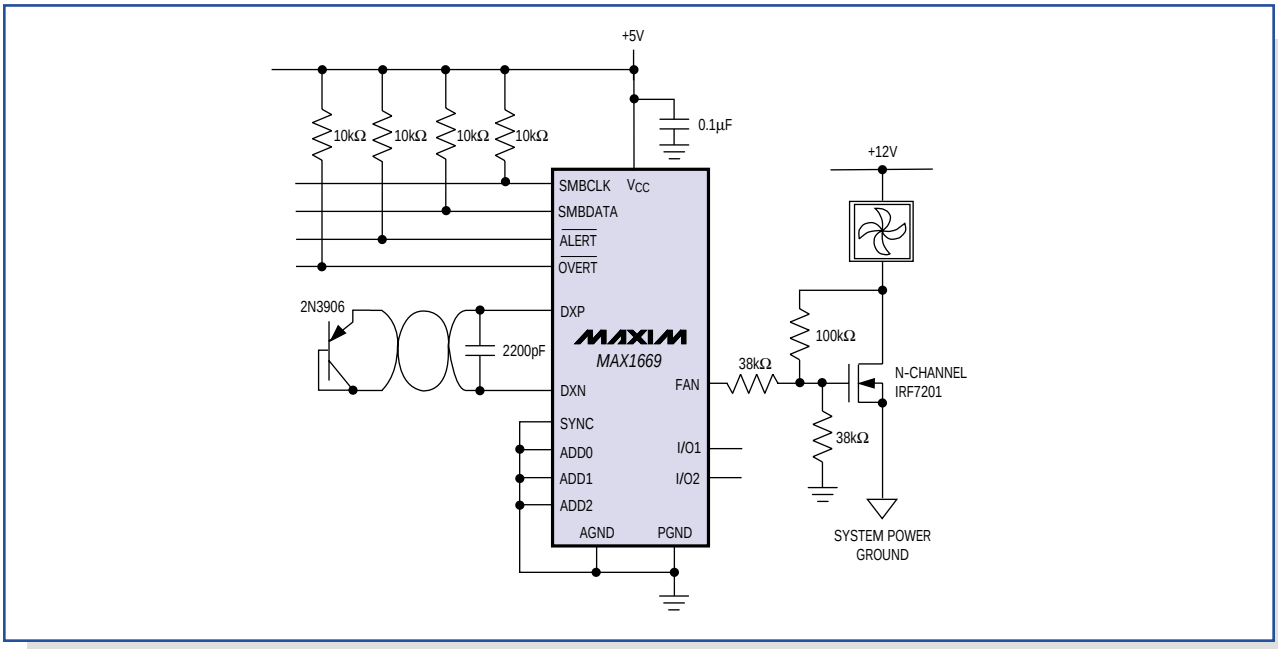


Figure 1. Typical circuit for linear control of a fan using the MAX1669.

regulating fan speed (**Figure 3**). This trades complexity along with the effort of designing the fan control amplifier. The feedback loop of the fan control amplifier contains both differentiation and integration, the time constants of which have to be found empirically for a given make and model of fan (once found, they can be fixed for production). This additional circuit adds cost with its higher component count.

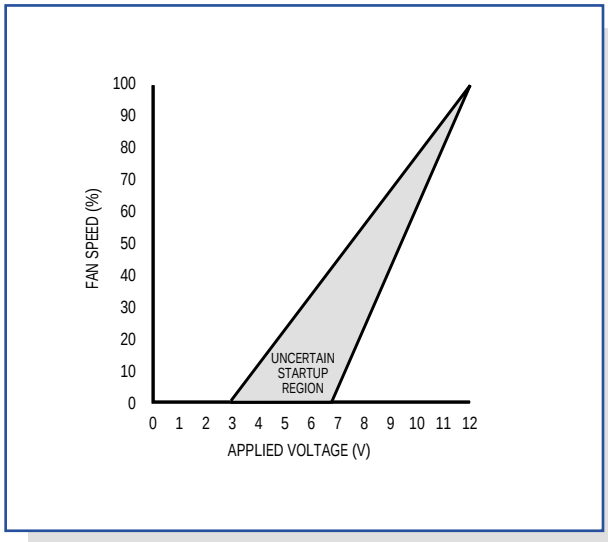


Figure 2. Typical fan speed vs. applied voltage.

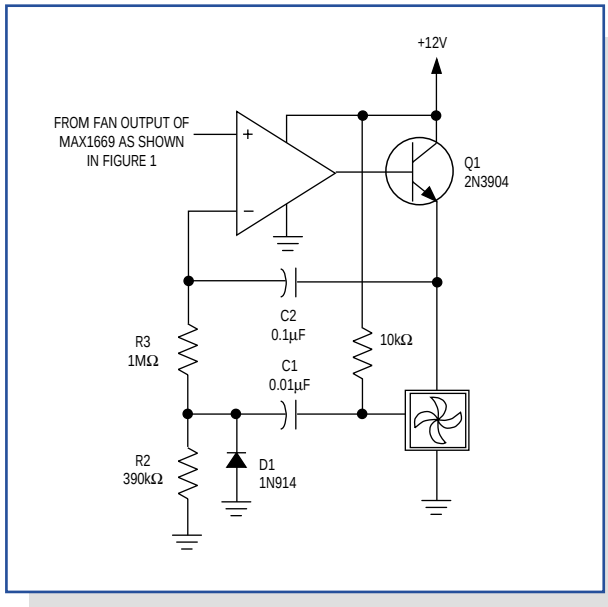


Figure 3. Using this fan control amplifier with the MAX1669 will provide full range, linear regulation (as opposed to fan control) of fans equipped with tachometer outputs.

Regulating fan speed

Maxim's newest fan controllers, the MAX6650 and MAX6651, make fan-speed regulation possible. The MAX6650/MAX6651 are closed-loop fan control ICs designed to accept feedback from the tachometer output of a fan. This makes programming fan speed straightforward without the user having to worry about startup or slow-speed reliability issues. Although both the MAX6650/MAX6651 can drive multiple fans (with tach feedback from only one of those fans), the MAX6651 can monitor the tachometer signals of up to four fans.

Figure 4 depicts a typical application for the MAX6650. The MAX6650 regulates fan speed based on a code programmed into its fan-speed register, by forcing the fan tachometer period to be equal to the scaled register value. Because typical fans produce two tachometer pulses per revolution, the required fan-speed register value is calculated as:

$$t_{TACH} = \frac{1}{2 \times \text{FanSpeed}} \quad (1)$$

$$K_{TACH} = \left[t_{TACH} \times K_{SCALE} \times \left(\frac{f_{CLK}}{128} \right) \right] - 1 \quad (2)$$

where:

K_{TACH} = Value programmed into the fan-speed register.

t_{TACH} = Period of the tachometer signal.

K_{SCALE} = Prescalar value (set in Configuration Register of the MAX6650/MAX6651 from 1 to 16 with a default of 4).

f_{CLK} = MAX6650/MAX6651 clock frequency (254kHz typ).

Other advantages of the MAX6650/MAX6651

The MAX6650/MAX6651 not only regulate fan speed, but also perform a wealth of other functions. There are watchdog functions that detect when the control loop is not regulating, when fan speeds are beyond programmed watchdog limits, and other general-purpose digital functions. Since these subjects are beyond the scope of this article, refer to the MAX6650/MAX6651 data sheet for details on all other functions.

The MAX6650/MAX6651 free the designer from the complex issues associated with the closed-loop amplifier

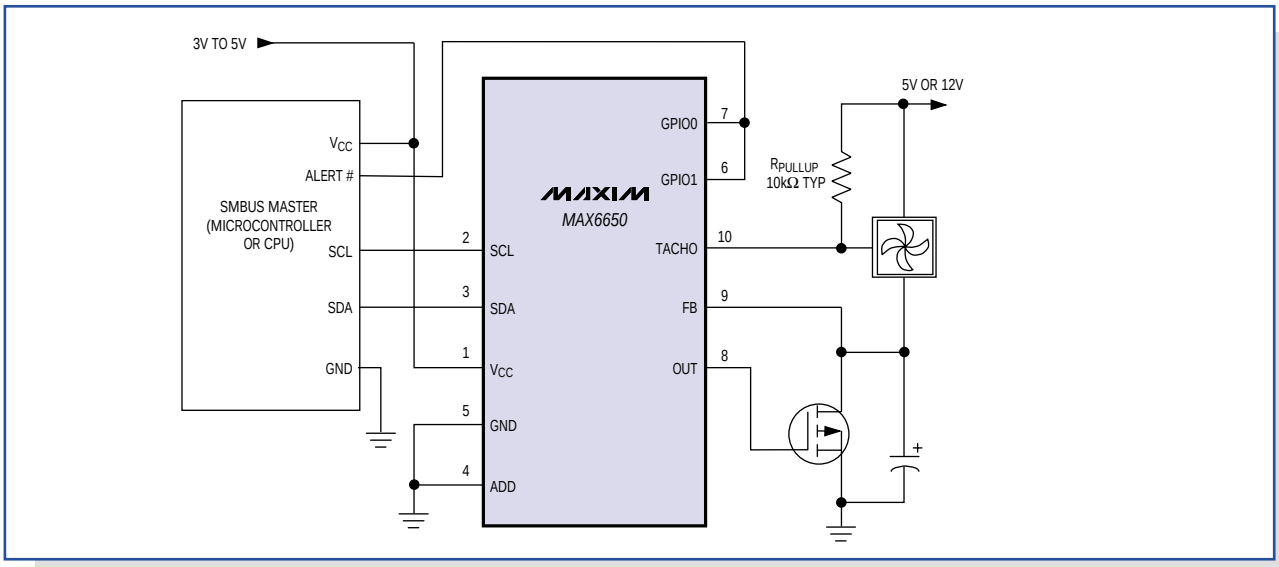


Figure 4. The MAX6650 is a true fan-speed regulator, by virtue of including a tachometer output fan in its feedback loop.

discussed previously, leaving only selection and installation of the pass transistor. Traditionally, a resistive-load, linear, control-pass element will be subject to maximum dissipation when delivering half the total supply voltage across the load. But does a resistive load represent a good model for fans? Modeling the fan as a resistive load would be more demanding than the actual real-world fan behavior would indicate. This suggests that conservative design practice can treat the fan as a resistive load with the only consequence being a choice of a larger pass transistor than might be used with careful fan characterization.

Take for example a fan that draws approximately 240mA at 12V. An equivalent resistance would consume 120mA at the half-voltage output point and correspond to a dissipation of 0.72W:

$$P_D = \frac{0.5V}{0.5I} = \frac{6}{0.12} = 0.72W \quad (3)$$

where PD represents worst-case resistive load dissipation.

If the following equation is satisfied, then no additional heatsinking is necessary:

$$\frac{T_{JMAX} - T_A}{P_D} \leq \varnothing_{J-A} \quad (4)$$

where:

T_{JMAX} = Maximum allowable junction temperature from transistor manufacturer's data sheet.

T_A = Maximum expected ambient temperature.

P_D = Power dissipation (same as Equation 3 above).

$\varnothing_{J-A}$ = Thermal resistance, junction to ambient, from transistor manufacturer's data sheet.

If the equation is not satisfied, a heatsink must be selected to satisfy the following:

$$R_{\varnothing SA} \leq \frac{T_{JMAX} - T_A}{P_D} - R_{\varnothing JC} \quad (5)$$

where:

$R_{\varnothing SA}$ = Heatsink thermal resistance (from heatsink manufacturer's data sheet).

$R_{\varnothing JC}$ = Pass transistor junction-to-case thermal resistance (from pass transistor manufacturer's data sheet).

The possibility of a total short circuit across the fan has not been discussed. If this happens, the full current available from the fan power supply will flow through the pass transistor. If this condition is a consideration, then that current and voltage value should be used in all the power dissipation and heatsinking calculations. Alternatively, current limiting circuitry could be included on the pass transistor, such as the circuit shown in **Figure 5**. Calculate the value of the current limit resistor according to:

$$R_{OUT} = \frac{0.6}{I_{LIMIT}} \quad (6)$$

where I_{LIMIT} is the desired value of current limit. Note that this current limit circuit is temperature sensitive. The 0.6 term in the equation is actually the base-emitter voltage of the current limit transistor which varies according to -2.2mV/°C. This can be useful as it acts to reduce the current limit as temperature rises.

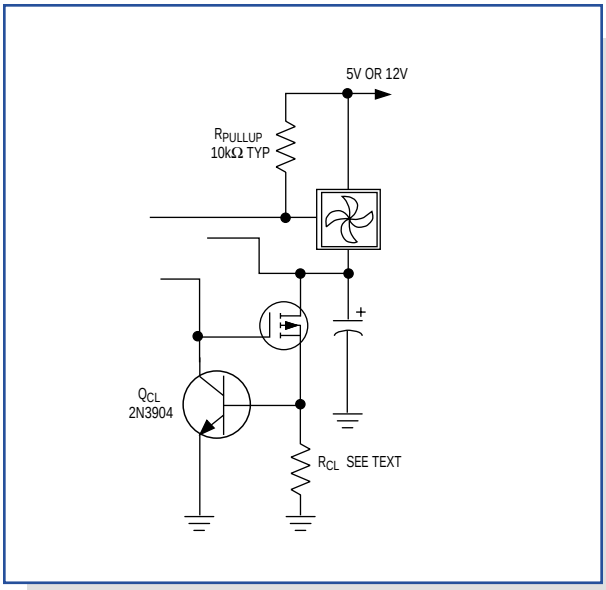


Figure 5. When current limiting is necessary for pass transistors, this circuit provides that function.

Optocoupler extends high-side current sensor to 1kV

Sensing DC current at high voltage is often problematic. Most off-the-shelf high-side current-sensing ICs have a stand-off voltage of 40V or less. Combining an optocoupler with such an IC yields a sensing circuit in which the high-side voltage is limited only by the optocoupler's stand-off voltage (**Figure 1**).

A precision, high-side current-sense amplifier (U1) and a high-linearity analog optocoupler (U3) extend the high-side working voltage to 1000VDC. U3 supports a continuous 1000VDC. Its UL rating is $5000V_{RMS}$ for one minute, and its transient surge rating is 8000VDC for 10 seconds. (Follow all proper safety precautions when working with high voltage.)

The circuit has a floating section and a grounded section, each requiring a local low-voltage supply. The floating section detects load current and drives the high-voltage side of the optocoupler. The grounded section monitors the optocoupler's low-voltage side and outputs a voltage proportional to the high-side load current. The chosen optocoupler has a feedback photodiode on the high-voltage side that virtually eliminates the LED's nonlinearity and drift characteristics. In addition, its two closely matched photodiodes ensure a linear transfer function across the isolation barrier.

During operation, the load current passes through shunt R1 and produces a small voltage. This voltage

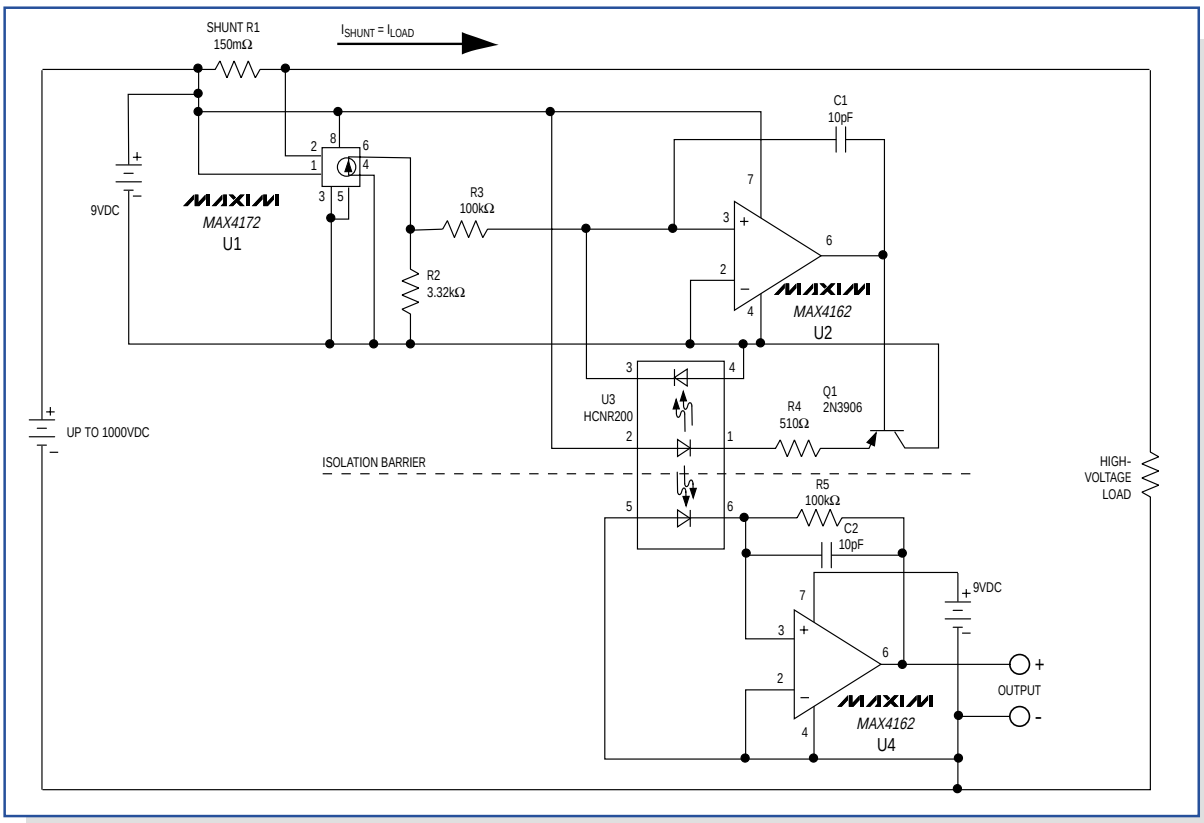


Figure 1. The ground-referenced output voltage $V_{OUT} = I_{SHUNT}$ (4.80V/A) is proportional to the high-side load current. As configured, the circuit measures load currents to 1A.

is monitored by U1, which outputs a proportional current of 10mA/V. This proportional output current is routed through R2, which produces a voltage proportional to the main load current. The rest of the circuit generates a copy of the voltage across R2, but on the low-voltage side of the optocoupler. U2 monitors the voltage across R2 and drives the opto-coupler's LED via Q1. Light generated by the LED impinges equally on the high-side and low-side photodiodes. U4 monitors the low-side photodiode and outputs a voltage proportional to the high-side load current. A graph shows the output voltage as a function of shunt current (**Figure 2**).

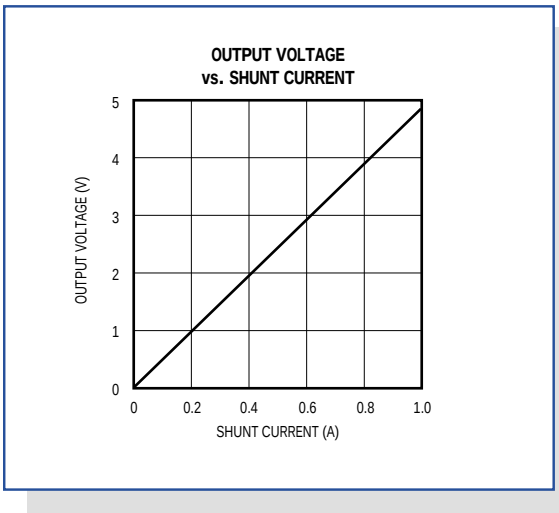


Figure 2. The output voltage vs. shunt current is linear for the design in Figure 1.

If R3 and R5 are equal in value, the overall transfer function is:

$$\frac{V_{OUT}}{I_{SHUNT}} = (0.01) \times (R1) \times (R2) \qquad (1)$$

Three parameters let you modify the circuit to monitor other maximum load currents and output a different voltage range. The maximum U1 output current is 1.5mA, so the maximum allowed shunt voltage is 150mV. Also, the maximum allowed photodiode current is 50µA. Choose an R1 value that produces 150mV at the maximum load current to be monitored. Then choose an R2 value that produces the desired corresponding maximum output voltage at 1.5mA. Match R3 and R5, choosing a value that allows less than 50µA through the photodiode at the maximum desired output voltage:

$$R3 \geq (V_{OUT\_MAX})/(50 \times 10^{-6}) \qquad (2)$$

The circuit output then faithfully reproduces the voltage across R2. The MAX4162 op amp was chosen for its low input bias current (1pA), Rail-to-Rail® input and output swings, and its ability to operate from a single 9V battery. With R1 = 150mΩ and R2 = 3.32kΩ as shown, the output voltage for I_{SHUNT} = 1A calculates to 4.80V using the transfer function above. Experimental results at I_{SHUNT} = 1.00A give V_{OUT} = 4.84V, with an error less than 1%.

Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.

Low-cost circuit breaker handles voltages to 32V

The simplicity of low-side current monitoring can mask the advantages of a high-side approach. You can monitor load currents in a power supply, motor driver, or other power circuit on either the high side or the low side (ground). Don't let the ease of low-side monitoring cause you to overlook the advantages of a high-side approach or the dangers of a low-side one. Various fault conditions can bypass the low-side monitor, subjecting the load to dangerous and undetected stresses.

On the other hand, a high-side monitor connected directly to the power source can detect any downstream failure and trigger the appropriate corrective action. Until recently, such monitors required a precision op amp, a boost power supply to accommodate the op amp's limited common-mode range, and a handful of precision resistors.

Today, a single IC (MAX4172) can sense high-side currents in the presence of common-mode voltages as high as 32V. Available in a tiny µMAX package, the MAX4172 provides a ground-referenced current-source output proportional to the high-side current of interest. This output current, which is numerically equal to the voltage across an external sense resistor divided by 100, can be applied across a load resistor to produce a simple voltage output.

The IC and a few low-cost external parts form a low-cost circuit breaker (**Figure 1**). Load currents are sensed by R_{SENSE} and controlled by Q1. The design accepts inputs between 10V and 32V and is easily modified to operate from voltages as low as 6.5V.

The initial application of V_{IN} and V_{CC} places the breaker in its tripped state. Pressing S1 resets the breaker and connects power to the load, which activates Q1, Q3, and Q4b. Q3 powers IC1, and Q4b establishes the overcurrent threshold

$$V_{THRESH} = V_{CC} - V_{be(Q4b)} \quad (1)$$

Because V_{CC} (2.7V to 5.5V typ) equals 5.0V and the base-emitter voltage of Q4b ($V_{be(Q4b)}$) is about 0.7V, V_{THRESH} is typically 4.3V. The circuit trips at a nominal load current of 1A.

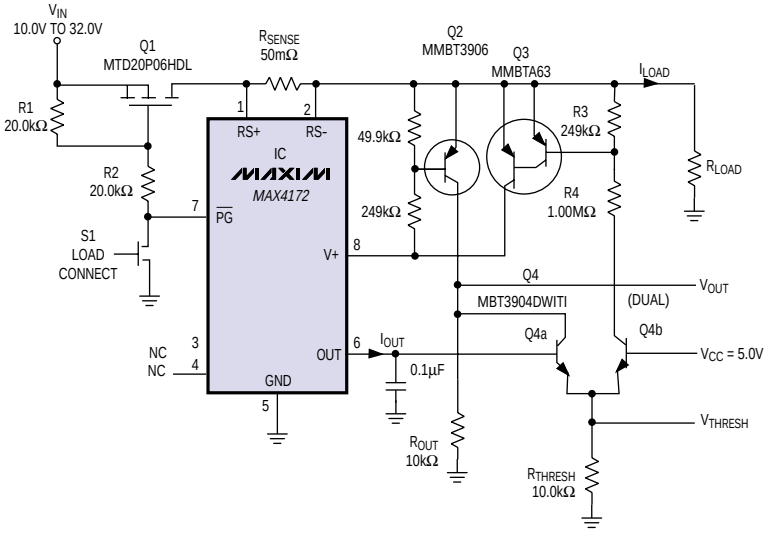


Figure 1. Configuring this current-sense amplifier and the transistors as shown provides a low-cost, high-voltage circuit breaker.

The values for R_{SENSE}, R_{THRESH}, and R_{OUT} are determined by the system's accuracy and power-dissipation requirements. First, select

$$R_{SENSE} = 50m\Omega \text{ and } R_{THRESH} = 10.0k\Omega \quad (2)$$

Then, calculate

$$R_{OUT} = V_{CC}/I_{LOAD}R_{SENSE}G_m \quad (3)$$

where I_{LOAD} = the trip point (1A), R_{SENSE} = 50mΩ, and G_m (the typical IC1 transconductance) equals 0.010A/V. Thus, R_{OUT} = 10.0kΩ.

Applying power to Q3 and Q4b causes Q4b to conduct, which establishes V_{THRESH} and activates Q3 to power IC1. A fraction of the load current through R_{SENSE} is mirrored to the IC1 output and observed as a voltage across R_{OUT} (V_{OUT}). Q4b turns off when V_{OUT} increases above (V_{THRESH} + $V_{be(Q4a)}$), turning off Q3 and causing a drop in V+ (IC1, pin 8). When V+ reaches 2.67V (typ), $\overline{PG}$ goes inactive (high), which trips the breaker by turning off Q1. Q2 adds feedback to ensure a clean turnoff at the trip level. Current draw in the tripped state is minuscule (unlike that of some current-interrupt devices). It equals the V_{CC} load current, which is 0.5mA typ.

Depress S1 to reset the breaker. (To automate, replace S1 with a transistor or open-drain comparator.) The design shown is intended for low-cost applications in which the absolute accuracy of trip current is not critical. This accuracy, which depends on variations in V_{CC}, variations in the V_{be} of Q4a and Q4b, and the error current through R4, is about ±15% at a parallel trip current of 1.0A.

Simple circuit provides reverse-battery correction

A universal problem in battery-operated devices is the threat of damage when the battery is inserted backwards by the end user (engineers never do this, of course). The error can be rectified by the use of a single diode or a diode-bridge configuration, but that fix wastes power and reduces the available voltage by adding one or two diode drops between the battery and the system supply rails.

An alternative solution not only protects against battery reversal, but also automatically corrects the reversal. To eliminate the voltage drops associated with discrete diodes, the MAX4636 has a low on-resistance, double-pole double-throw (DPDT) analog switch (U1) configured as a full-wave rectifier (**Figure 1**).

When the battery is inserted with correct polarity as shown, the upper switch (S1) is in its normally closed state (as shown) because its control input (pin 1) is low. The resulting connection from pin 2 to pin 10 provides a low-impedance path from the battery to the V_{CC} output. Conversely, the lower switch (S2) closes its normally open terminal (not shown) because its control input (pin 5) is high. The resulting path from pin 7 to pin 6 connects the battery's negative terminal to ground.

Startup is guaranteed by the ESD diodes internal to U1, which also act as a full-wave rectifier. MOSFETs inside the analog switch turn on when the battery voltage exceeds 1V. Their extremely fast operation (turn-on is less than 20ns) enables the circuit to maintain normal operation by quickly swapping the leads of a reversed-polarity battery connection.

Circuit resistance is proportional to the battery voltage. When operating with four NiCd, NiMH, or alkaline cells, the resistance from each side of the rectifier is 2.5Ω (5Ω total). Operation with a 2-cell battery (2.4V to 3V) produces a total resistance of 10Ω.

U1 is rated for operation up to 5.5V and 30mA continuous current, making the circuit useful for cordless phones, portable audio equipment, handheld electronics, and other light- to medium-current applications. U1's ultra-miniature 10-pin µMAX package occupies less space than four through-hole signal diodes, and is almost as small as the two SOT23 dual-signal diodes required in implementing a discrete-diode alternative.

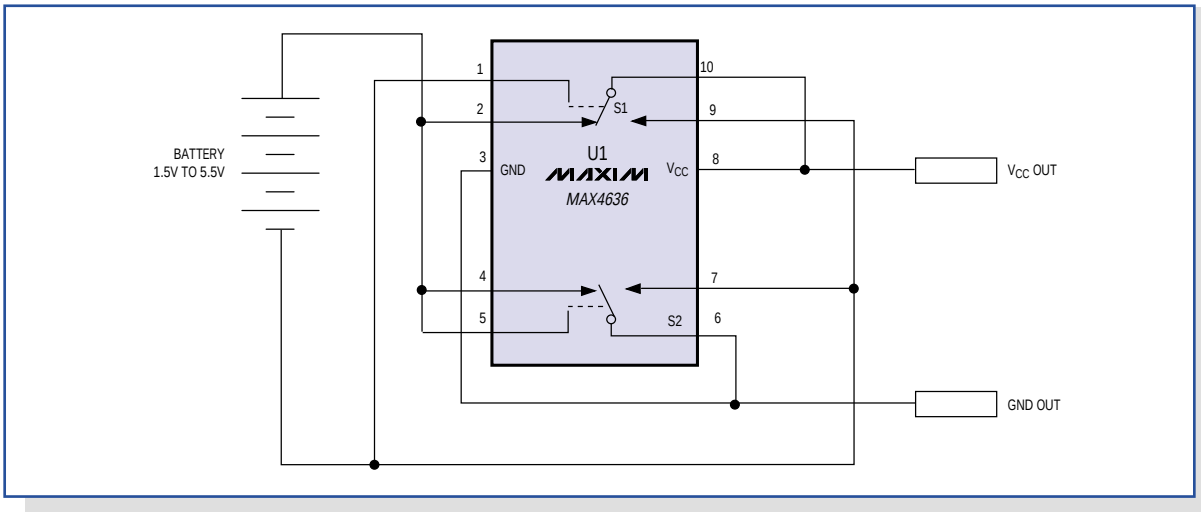


Figure 1. The connections shown enable this fast analog switch to sense the battery polarity and then quickly connect the load or swap leads first.

Single-chip FM transmitter extends home-entertainment systems

A simple FM transmitter (**Figure 1**) links your home-entertainment system to a portable radio that can be carried around the house and into the backyard. For example, you can play music on the CD changer in your living room and listen to it on a portable radio by the backyard barbeque.

IC1 is a voltage-controlled oscillator with integrated varactor. Its nominal oscillation frequency is set by inductor L1, and a 390nH value places that frequency at 100MHz. Potentiometer R1 then lets you select a channel by tuning over the FM band of 88MHz to 108MHz. Output power is about -21dBm into 50Ω (most countries accept emissions below 10dBm in the FM band).

The home system's left and right audio signals are summed by R3 and R4, and attenuated by the (optional) potentiometer R2. R2's wiper signal serves as a volume control by modulating the RF frequency. Signals above 60mV introduce distortion, so the pot attenuates down from that level.

In the absence of a standard FM radio antenna, 75cm of wire will suffice as a transmitting antenna. For best reception, it should be mounted parallel with the receiving antenna. The IC operates on a single-supply voltage in the 3V to 5V range, but you should regulate the applied voltage to minimize frequency drift and noise.

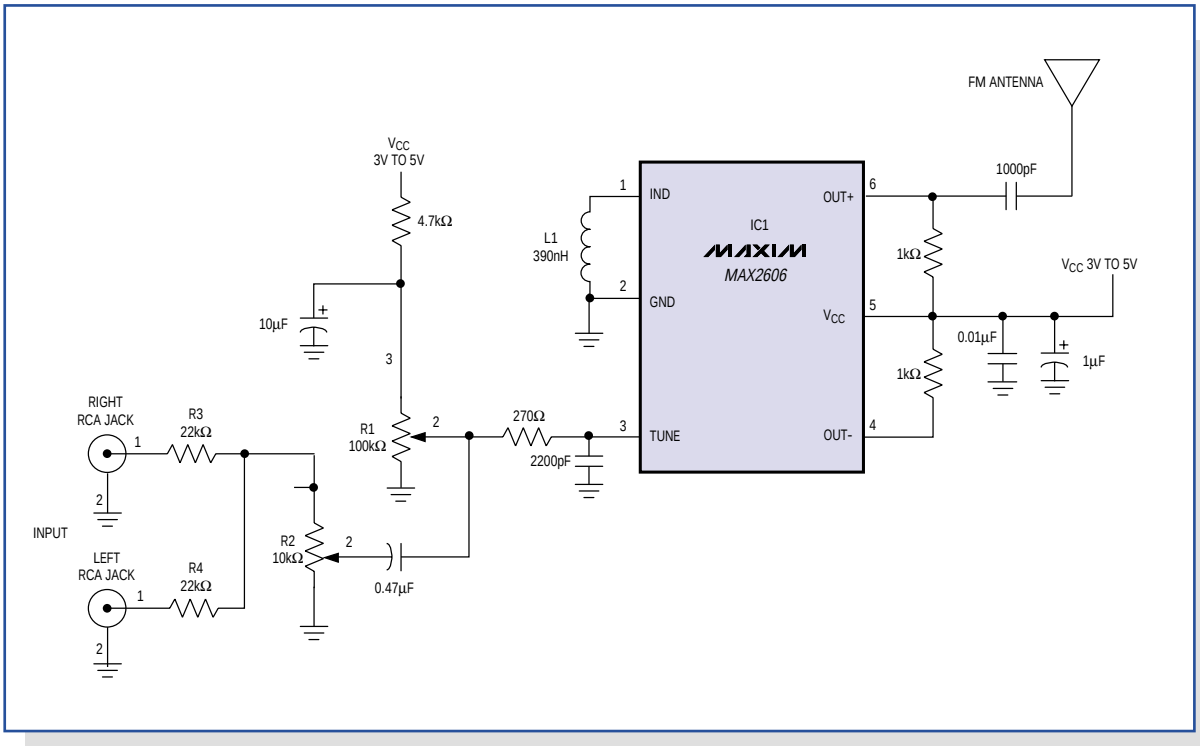


Figure 1. This simple, short-range FM radio transmitter has only one IC.

Emitter follower boosts linear regulator's output current

Automotive electronics often require memory for saving system information or for user inputs (the settings on a car stereo, for example). Flash memory can do the job, but flash is expensive. DRAM memory reduces the cost, but DRAM requires an always-on power supply. A standard linear regulator such as the LM78L05 can generate the 5V rail required for 5V DRAM, but its supply current (as much as 5mA) can discharge the battery over an extended period of inactivity.

Conversely, linear regulators with low quiescent current may not have sufficient load-current capability to supply the DRAM during active read or write operations. The solution is to add an emitter-follower output stage to a low-current, high-voltage, low-dropout (LDO) regulator (**Figure 1**). Adding the transistor as shown, between the LDO output and load, increases the available output current without increasing the regulator's low (15µA) quiescent current.

Though not an issue for the application in question (regulating a 12V battery down to 5V), the dropout voltage for this circuit (minimum-allowed V_{IN} minus V_{OUT}) equals that of the regulator IC (350mV max) plus the transistor's base-emitter drop of approximately 0.7V. The pass element in IC1 is a PNP transistor whose saturation at low dropout voltage increases the quiescent current for that condition. To maintain low quiescent current, therefore, the regulator headroom should be kept well above 1V.

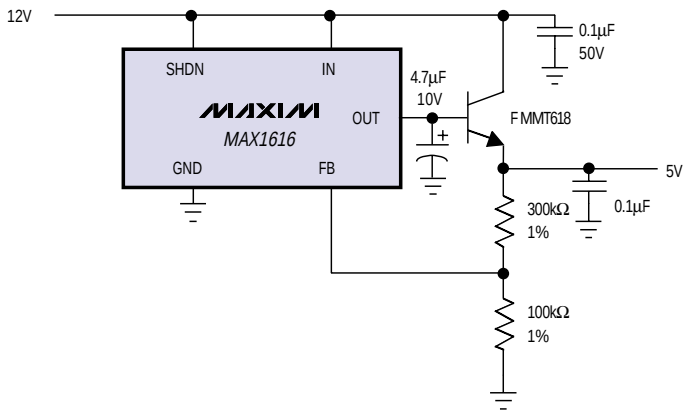


Figure 1. An external emitter follower increases the output current while maintaining the low quiescent current of this LDO regulator.